

**REMARKS**

Claims 1-5 are pending in this application, of which claims 1, 4 and 5 have been amended. No new claims have been added.

The references disclosed in the specification are properly included and cited in a Supplemental IDS, attached hereto. The specification has been amended on page 10 to properly cite the reference referred to as "SSDM". A concise English translation of document AF first presented in the IDS filed June 4, 2001 is included in this attached Supplemental IDS.

The Examiner has objected to claim 1 for an informality which has been corrected in the aforementioned amendments.

Claims 1-5 stand rejected under 35 USC §112, first paragraph, for failing to provide a disclosure enabling one of ordinary skill in the art to make and/or use the invention. In particular, the Examiner urges that claim 1 is non-enabled because it is not clear to the Examiner how "power supplied to a load is at least partially collected to said charge recycle power source". The Examiner urges that the specification fails to provide an adequate explanation of how this step is being performed.

In response, please refer to Figs. 3-6 and the related description in the specification.

The power supply to a load is collected by a charge recycle power source, because the power source has capacitors which store charges returned from the load. The collection of charge itself from a load to a power source is described in JP 8-335873, and the reference cited on page 10, line 3 of the specification of the instant application.

However, JP 8-335873 and this reference concern a combination logic circuit, but not a clock

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signal in a register circuit. Further, those references must use a specific circuit, therefore, they are not compatible with a conventional CMOS circuit. Further, they do not show the inequality recited in claim 1 of the present invention.

As compared with the claim 1 of the present application with those references, the present invention is directed to decrease power consumption in a clock signal. The present invention can also use a conventional register circuit (CMOS circuit), therefore, the present invention is compatible with a conventional CMOS circuit, in other words, a conventional CMOS register circuit can operate with low power consumption merely by replacing a clock power source to the present clock power source. The present invention satisfies the inequality in claim 1, which prevents leak current due to the characteristic of gradual charging of adiabatic logic, so that power consumption in a clock signal can be decreased even 1/10 as compared with that of a prior art.

Thus, the 35 USC §112, first paragraph, rejection should be withdrawn.

Claims 1-5 stand rejected under 35 USC §112, second paragraph, as indefinite.

Accordingly, claims 1 and 4-5 have been amended to correct the noted instances of indefiniteness, and the 35 USC §112, second paragraph, rejection should be withdrawn.

Claims 1-3 and 5 stand rejected under 35 USC §103(a) as unpatentable over U.S. Patent 5,994,935 to Ueda et al. (hereinafter "Ueda et al.") in view of Applicants' Admitted Prior Art (hereinafter "APA").

Applicants respectfully traverse this rejection.

Ueda et al. discloses a flip-flop circuit constituted by two latch circuits of the same structure that are cascaded. The latch circuit each includes an inverter formed of a P channel transistor and

an N channel transistor, an N channel transistor connected between a common node and a ground node, and two data input/output terminals. Two kinds of clock signals supplied to gates of N channel transistors are complementary to each other.

The Examiner has urged that Ueda et al. does not disclose a charge recycle power source to generate the clock signal, but has cited APA on page 10, lines 1-3 for teaching that "it is well-known that waveform generator 30 ... can be used to generate the power clock signal in which power supplied to a load is partially collected and returned to the charge recycle power source, and the inequality ( $|V_{TN}| + |V_{TP}| \geq VDD$ ) is satisfied."

Applicants respectfully disagree. The portion of the specification referred to by the Examiner as APA does not, in fact, discuss prior art. This passage instead discloses the present invention.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-5, as amended, are in condition for allowance, which action, at an early date, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an

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appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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                  Substitute Abstract of the Disclosure  
                  Substitute Specification  
                  Marked-up Specification

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**IN THE ABSTRACT:**

Amend the Abstract as follows:

An adiabatic charging register circuit [comprising] including a plurality of n-channel MOSFET's and a plurality of p-channel MOSFET's, is operated by a clock signal which has a gradually rising and a gradually falling waveform generated by using a charge recycle power source in which charge supplied to a load is at least partially collected to said charge recycle power source, and following inequality is satisfied;

$$\left| V_{TN} \right| + \left| V_{TP} \right| \geq VDD$$

where  $V_{TN}$  is threshold of an n-channel MOSFET,  $V_{TP}$  is threshold of a p-channel MOSFET, and VDD is output voltage of said charge recycle power source.

[(Fig.4)]

**IN THE CLAIMS:**

Please amend claims 1, 4 and 5 as follows:

1. (Amended) A register circuit having a plurality of n-channel MOSFET transistors and a plurality of p-channel MOSFET transistors, accepting an input data, and a clock signal, and providing an output data,

said clock signal being a power clock signal having a [gradually] rising and gradually falling waveform generated by using a charge recycle power source in which power supplied to a load is at least partially collected and returned to said charge recycle power source, and

the following inequality is satisfied[;]:

$$|V_{TN}| + |V_{TP}| \geq VDD$$

[here] where  $V_{TN}$  is a threshold of said n-channel MOSFET transistor,  $V_{TP}$  is a threshold of said p-channel MOSFET, and  $VDD$  is an output voltage of said charge recycle power source.

4. (Amended) A register circuit according to claim [1] 2, wherein said register circuit includes a combination logic circuit between said pair of D-latch circuits.

5. (Amended) A register circuit according to claim [1] 2, wherein said D-latch circuit comprises a memory element having a first inverter providing an output of the D-latch circuit, a second inverter with an input coupled with an output of said first inverter, and a first transmission gate connecting an output of the second inverter to an input of the first inverter, and a second transmission gate inserted between an input terminal and an input of said first inverter.



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## BACKGROUND OF THE INVENTION

*1. Field of the Invention*  
The present invention relates to an adiabatic charging register circuit, in particular, relates to such a circuit which reduces power consumption associated with a clock pulse.

*2. Description of the Related Art*  
Conventionally, an LSI circuit includes a large number of register circuits, fifty [thousands] <sup>thousands</sup> or more circuits. Each register circuit comprises a D-flip flop (D-FF) or D-latch circuit. A register circuit having a D-FF or D-latch is exemplified here.

First, a register circuit having a D-FF is described.

A D-FF has a pair of D-latch circuits. Fig.17 shows an example of a D-latch circuit (page 677, "Structure of Design of a Computer" <sup>Computer</sup> by Paterson, <sup>David Patterson</sup> and Henesey, <sup>John L. Henesey</sup> published by NikkeiBP). A D-latch circuit 70 in Fig.17 has a pair of NOR circuits 71 and 72 which are cross-connected to each other constituting a RS-FF (reset-set-flip-flop), and a pair of AND circuits 73 and 74. It has data input terminals D, DN in differential form, a clock input terminal CK, and data output terminals Q, QN in differential form. Each of NOR circuits 71 and 72 operates as an inverter when one of the inputs of the same is in low state, and therefore, a D-latch circuit 70 in Fig.17 operates as follows.

(1) A pair of NOR circuits 71, 72 keep a previous state when a clock input terminal CK is in low state.

(2) A value of a data input terminal D is stored in a pair of NOR circuits 71, 72 when a clock input terminal CK is in high state.

A D-FF circuit 80 is constituted by using a pair of D-latch circuits 70 as shown in Fig.18, in which a first stage D-latch circuit 70A receives a clock input CK as it is, and a

second stage D-latch circuit 70B receives a clock signal which is inversion by  $180^\circ$  of the clock input CK by an inverter 90. A D-FF circuit operates as follows.

(1) When a clock input CK becomes <sup>to</sup> high state, the first stage D-latch circuit 70A opens to accept a data D at an input terminal,

(2) When a clock input CK becomes <sup>to</sup> low state, the second stage D-latch circuit 70B opens and an input terminal D accepts an output O1 on an output terminal Q of the first stage D-latch 70A, as an input signal D.

Fig.19 shows operational wave forms of a data D, a clock input CK, an output O1 of the first stage D-latch circuit 70A, and an output O2 of the second stage D-latch circuit 70B. As shown in Fig.19, the output O2 is switched by an input data when a clock input CK is switched from high state to low state, thus, it is an edge trigger type circuit.

Conventionally, a clock signal CK is generated by using an inverter having a CMOS circuit which has a p-channel MOSFET and an n-channel MOSFET connected in series <sup>with</sup> each other, and has rectangular wave form. A load coupled with an output of a clock signal generator is charged to power supply voltage VDD through p-channel MOSFET of an inverter when an output signal is in high state, and is discharged to ground through n-channel MOSFET of an inverter when an output signal is in low state. Therefore, the power consumption P by a clock signal is  $P = CV^2f$ , where f is <sup>the</sup> clock frequency, V is <sup>the</sup> power supply voltage, and C is <sup>the</sup> sum of capacitance of wires and gate capacitance which accept a clock signal.

The capacitance of wires is <sup>recently</sup> large because of increase of semiconductor chip area of an integrated circuit reflecting



a large scale integrated circuit, and therefore, power consumption by charge/discharge of a clock signal occupies almost 50% of the total power consumption of a semiconductor chip (page 90, Technical Report of <sup>Low power</sup> LSI, Nikkei Micro-device, NikkeiBP).

Further, a large number of register circuits are used for a pipeline processing in an LSI for processing <sup>2</sup> moving image, and a RISC processor. In those devices, it is also known that power consumption by a clock system is almost the same as that by a logic system (page 8, Low power and high speed LSI technology, Realize Co.). That relation is independent from operation speed, but depends upon <sup>1</sup> ratio occupied by a register circuit in an LSI.

#### SUMMARY OF THE INVENTION

It is an object, therefore, of the present invention to provide a new and improved register circuit by overcoming the disadvantages and limitations of a prior register circuit.

It is also an object of the present invention to provide a register circuit which consumes less power in a clock system.

It is further an object of the present invention to provide a register circuit in which no short-circuit current from a power source to ground directly flows.

The above and other objects are attained by an adiabatic register circuit comprising; a plurality of n-channel MOSFET transistors and a plurality of p-channel MOSFET transistors, accepting an input data, and a clock signal, and providing an output data; said clock signal being a power clock signal having a gradually rising and gradually falling waveform generated by using a charge recycle power source in which power supplied to a load is at least partially collected <sup>and recycled</sup> to said charge recycle

power source; and

following inequality is satisfied;

$$|V_{TN}| + |V_{TP}| \geq VDD$$

where  $V_{TN}$  is threshold of said n-channel MOSFET transistor,  $V_{TP}$  is threshold of said p-channel MOSFET, and VDD is output voltage of said charge recycle power source.

1 [Preferable] ~~Preferably~~ said register circuit comprises a pair of D-latch circuits with an input of a second D-latch circuit coupled with an output of a first D-latch circuit, a first D-latch circuit accepts a first power clock signal, and a second D-latch circuit accepts a second power clock signal which is different by 180° of the first power clock signal.

Preferably, said D-latch circuit comprises a pair of NOR circuits with one of the inputs of each NOR circuit being coupled with an output of the other NOR circuit, and a pair of AND circuits each accepting an input data in differential form and a power clock signal, and providing an output to the other input of each of said NOR circuit.

Preferably, said register circuit includes a combination logic circuit between said pair of D-latch circuits.

Preferably, said D-latch circuit comprises a memory element having a first inverter providing an output of the D-latch circuit, a second inverter with an input coupled with an output of said first inverter, and a first transmission gate connecting an output of the second inverter to an input of the first inverter, and a second transmission gate inserted between an input terminal and an input of said first inverter.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features, and attendant

advantages of the present invention will be appreciated as the same become better understood by means of the following description and drawings wherein;

Fig.1 is a block diagram of a D-FF circuit according to the present invention,

Fig.2A is a circuit diagram of a D-latch circuit used in the D-FF circuit in Fig.1,

Fig.2B shows a transistor circuit of a D-latch circuit in Fig.2A,

Fig.2C shows operation of a conventional CMOS inverter,

Fig.3 is a circuit diagram of a gradually rising and gradually falling waveform generator,

Fig.4 shows waveforms of a power clock used in a D-FF circuit in Fig.1,

Fig.5 shows waveforms of another power clock used in a D-FF circuit in Fig.1,

Fig.6 shows waveforms of still another power clock used in a D-FF circuit in Fig.1,

Fig.7 shows operational waveforms of a D-FF circuit in Fig.1,

Fig.8 shows simulation result of a D-FF circuit using a conventional rectangular clock,

Fig.9 shows simulation result of a D-FF circuit using the present power clock,

Fig.10 is a block diagram of a logic system having an alternate arrangement of a D-FF circuit in Fig.1 and a logic circuit,

Fig.11 is a block diagram of another logic system having an alternate arrangement of a D-latch circuit in Fig.1 and a logic circuit,

Fig.12 is a modification of Fig.11, and shows a pair of D-latch circuits coupled directly with no logic circuit between them,

Fig.13 shows operational waveforms of a circuit of Fig.12,

Fig.14 is another embodiment of a D-latch circuit using a transmission gate,

Fig.15 shows waveforms of a power clock used in a circuit of Fig.14,

Fig.16 shows the effect of the present invention,

Fig.17 is a prior D-latch circuit,

Fig.18 is a prior D-FF circuit, and

Fig.19 shows operational waveforms of a D-FF circuit in Fig.18.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to the present invention, a clock signal is a charge recycle type power clock generated by using a charge recycle power source, and having a gradually rising and gradually falling waveform, while a conventional clock signal use a rectangular clock signal. A register circuit using such a power clock signal has the advantage that power consumption in a clock system is considerably reduced as compared with that of a prior art, for instance, it is reduced to 1/10 of that of a prior art. Further, when an n-channel MOSFET and a p-channel MOSFET which constitute a register circuit satisfy the following condition, no short-circuit current from a power source to ground is allowed;

$$|V_{TN}| + |V_{TP}| \geq VDD$$

where  $V_{TN}$  is threshold of an n-channel MOSFET,  $V_{TP}$  is threshold of a p-channel MOSFET,  $VDD$  is output voltage of a power source.

(First Embodiment)

Fig.1 is a block diagram of a D-FF circuit 20 which is a first embodiment of the present invention. The D-FF circuit 20 comprises a first stage D-latch circuit 10A, and a second stage D-latch circuit 10B. Each of the D-latch circuits 10A and 10B is shown in Fig.2A by the reference numeral 10, which comprises a pair of NOR gates 11 and 12 conforming an RS-FF, and a pair of AND gates 13 and 14.

A The circuit of Fig.2A is implemented by a CMOS including a p-channel MOSFET and an n-channel MOSFET, as shown in Fig.2B, in which an AND circuit and a NOR circuit are implemented by three p-channel MOSFET's and three n-channel MOSFET's as shown in the figure. Thus, the structure of Fig.2A is implemented by using two sets of a circuit of Fig.2B.

Now, a short-circuit current flowing from a power source VDD to ground directly in a CMOS circuit is analyzed in accordance with Fig.2C. In an inverter having a series circuit of a p-channel MOSFET and an n-channel MOSFET between a power source VDD and a ground, a short-circuit current from a power source VDD to ground flows during transient time of an input signal. As a power clock rises and falls slowly, a short-circuit current during transient time would be larger than that of a prior art which uses a prior rectangular clock. The upper portion of Fig.2C shows the relation between an input voltage IN and an output voltage OUT, and the lower portion of Fig.2C shows the relation between an input voltage IN and a short-circuit current. The maximum short-circuit current I<sub>max</sub> is:

$$I_{\max} = (\beta_n / 2) ((V_{DD} - |V_{TN}| - |V_{TP}|) / (1 + \sqrt{\beta_n / \beta_p}))^2$$

$$V_{DD} > |V_{TN}| + |V_{TP}|$$

$$I_{\max} = 0$$

$$VDD \leq |V_{TN}| + |V_{TP}|$$

where  $\beta_n = \mu_n C_{ox}(W/L)$

$\mu_n$  is mobility

W is channel width of a MOSFET

L is channel length of a MOSFET

$C_{ox}$  is oxide capacitance per unit area

Therefore, a short-circuit current from a power source to ground is zero, even if a gradually rising and gradually falling power clock is used, when  $VDD \leq |V_{TN}| + |V_{TP}|$  is satisfied.

According to the present invention, a threshold value  $V_{TN}$  of an n-channel MOSFET and a threshold value  $V_{TP}$  of a p-channel MOSFET is designed high so that the following inequality is satisfied;

$$|V_{TN}| + |V_{TP}| \geq VDD$$

where  $V_{TN}$  is a threshold of an n-channel MOSFET used in NOR gates 11 and 12, and AND gates 13 and 14,  $V_{TP}$  is a threshold of a p-channel MOSFET used in NOR gates 11 and 12, and AND gates 13 and 14, and VDD is power source voltage. That condition allows no short-circuit current from a power source to ground of a logic gate in a D-latch circuit 10.

Further, according to the present invention, a clock input terminal PCK of a first stage D-latch circuit 10A in a D-FF 20 receives a first power clock PCK1 which is generated by a charge recycle type power source, and has wave-form which rises and falls slowly or gradually, and a clock input terminal PCK of a second stage D-latch circuit 10B in a D-FF 20 receives a second power clock PCK2 which [has] different phase by  $180^\circ$  of that of the first power clock PCK1.

The power clocks PCK1 and PCK2 may be generated by using

a gradually rising and gradually falling waveform generator 30 constituted by a switched capacitor circuit as shown in Fig.3 (1999 SSDM page 444), or an LC resonance circuit (not shown). In Fig.3,  $T_0 - T_4$ ,  $T_0' - T_4'$  are a transmission gate,  $C_1 - C_3$  are a capacitor. A gradually rising and gradually falling waveform generator 30 provides a pair of power clocks PCK1 and PCK2 having a gradually rising and gradually falling waveform by conducting a pair of transmission gates sequentially in the following sequence.

$(T_0, T_0') \rightarrow (T_1, T_1') \rightarrow (T_2, T_2') \rightarrow (T_3, T_3') \rightarrow (T_4, T_4') \rightarrow (T_3, T_3') \rightarrow (T_2, T_2') \rightarrow (T_1, T_1') \rightarrow (T_0, T_0') \rightarrow (T_1, T_1') \rightarrow$

Assuming that  $V_{DD}=1V$ ,  $|V_{TN}| = |V_{TP}| = 0.7V$ , the operation of the first stage D-latch circuit 10A and the second stage D-latch circuit 10B is shown in Fig.4. When the amplitude of the power clocks PCK1 and PCK2 is higher than 0.7V, the D-latch circuit 10A or 10B accepts an input data, and keeps the previous status when the amplitude of the power clocks PCK1 and PCK2 is lower than 0.7V.

Figs.5 and 6 show wave-forms of power clocks PCK1 and PCK2 having different duty ratio from each other.

In those figures, the period  $T_{FF}$  shows the time from data input to data output in a D-FF circuit 20, and the period  $T_{combination}$  shows the allowable delay time allowed to a combination logic circuit coupled with an output or an input of a D-FF circuit 20.

A D-FF circuit driven by power clocks PCK1 and PCK2 is called an adiabatic charging D-FF circuit, (since power consumption of power clocks are not consumed but are returned to a power supply. The adiabatic charging D-FF circuit has the following features.

- (1) It has cross-wired NOR gates in static operation which

is stable as compared with dynamic operation. Static operation has an output equal to VDD or 0, while dynamic operation has not only an output of VDD or 0, but also an open output which is not VDD nor 0.

(2) No data goes directly from input to output of a D-FF circuit, [since] a first stage D-latch 10A and a second stage D-latch 10B do not take data simultaneously.

(3) Both D-latch circuits 10A and 10B have a period of storage mode simultaneously. In that case, each D-latch circuit 10A and 10B stores data independently.

(4) The time  $T_{FF}$  is larger than  $T_{FF}$  of a prior D-FF circuit.

(5) The power consumption is less than 1/10 of that using a conventional rectangular clock signal, [since] power clocks PCK1 and PCK2 are used.

(6) It is compatible with a prior D-FF. In other words, a conventional D-FF circuit constituted by a CMOS circuit using a rectangular clock signal can be substituted with an adiabatic charging D-FF circuit using a charge recycle type power source.

Fig.7 shows the operation of an adiabatic charging D-FF circuit of Fig.1. It is noted that an input data D is taken when a power clock PCK1 changes from high to low, and the data thus taken is kept for a period of the PCK2 (see an output wave form 02).

Figs.8 and 9 show the simulation result using a simulation software HSPICE. Fig.8 shows the result of a conventional D-FF 80 in Fig.18 when a conventional rectangular clock CK is used, and Fig.9 shows the result of the present D-FF 20 in Fig.1 when the present power clocks PCK1 and PCK2 are used. The power clock PCK2 is not shown [since] it is the same as PCK1 but different phase by 180° phase. In the simulation, it is assumed that the



gate length of an n-channel MOSFET and a P-channel MOSFET is  $0.25\ \mu\text{m}$ , the gate width of a p-channel MOSFET is  $9\ \mu\text{m}$ , the gate width of an n-channel MOSFET is  $6\ \mu\text{m}$ , the threshold is  $|V_{\text{TN}}| = |V_{\text{TP}}| = 0.3\text{V}$ , the power supply voltage is  $V_{\text{DD}} = 0.5\text{ V}$ , and the period of a clock signal (PCK1, PCK2, CK) is  $100\text{ nS}$  ( $f = 10\text{ MHz}$ ).

The simulation result shows that outputs of a D-FF circuit when PCK1 and PCK2 are used are the same as those when a conventional clock CK is used.

A The power consumption by a D-FF circuit with a constant power supply voltage is  $320\text{ nW}$  in both a conventional D-FF circuit using a CMOS, and the present adiabatic charging type D-FF circuit. No increase in power consumption by a short-circuit current occurs as no short-circuit current flows. The power consumption by a conventional rectangular clock signal CK is  $310\text{ nW}$ , while the power consumption by the present power clock signals PCK1 and PCK2 is only  $23\text{ nW}$ . Thus, [the] power consumption by the adiabatic power clock signals is less than  $1/10$  [of] that of a conventional clock signal.

19 Fig.10 shows a logic system having<sup>22</sup> alternate arrangement of a D-FF circuit 20A through 20C of the D-FF circuit 20 in Fig.1, and combination logic circuit 40A through 40C. It should be noted that the process time in a logic circuit 40A through 40C is less than said  $T_{\text{combination}}$ .

(Second embodiment)

24 Fig.11 shows<sup>23</sup> (the) second embodiment according to the present invention. The feature of Fig.11 is an alternate arrangement of a D-latch circuit 10A through 10D of the D-latch circuit in Fig.2 and a combination logic circuit 40A through 40D. No concept of the time  $T_{\text{FF}}$  exists in this embodiment, and the

allowable delay time allowed to each combination logic circuit 40A through 40D is the same as the allowed time between latch circuits using a conventional rectangular clock signal.

Fig.12 is a modification of Fig.11. In Fig.12, a pair of D-latch circuits 10A and 10B are coupled directly together with no combination logic circuit between the D-latch circuits, and the operational wave forms of Fig.12 are shown in Fig.13, which is almost the same as those of Fig.7 which shows the operation of Fig.1, except that an input data I is slightly modified so that an input data I changes from high to low at time  $t_1$  when a power clock PCK1 is higher than threshold value, the wave form of the input signal I appears in an output O1.

(Third embodiment)

Fig.14 shows the third embodiment according to the present invention. In this embodiment, a latch circuit is comprised of a memory circuit having a pair of inverters 60A and 60B, and a transmission gate 50B, and another transmission gate 50A connected to an input side of the transmission gate 50B. Four power clocks PCK1, PCK2, PCK3 and PCK4 are used. PCK1 and PCK2 are applied to the transmission gate 50A, and have the opposite relations with each other. PCK3 and PCK4 are applied to the transmission gate 50B, and have the opposite relations with each other. PCK1 and PCK2 are shifted by  $180^\circ$  from PCK3 and PCK4, respectively.

Fig.15 shows wave forms of power clocks PCK1 through PCK4.

(Consideration of a D-latch circuit)

Two kinds of D-latch circuits are possible, one is an RS-FF type as shown in Fig.2, and the other is a transmission gate

type as shown in Fig.14.

2 An RS-FF type takes static operation for input and storage of a data, and operates correctly even for slow speed operation. On the other hand, a transmission gate type circuit operates dynamically, and is not suitable <sup>to</sup> very slow speed operation.

u As for a number of transistors which receive a clock signal, an RS-FF type circuit has four transistors (two transistors in each AND gate), and a transmission gate type circuit has six transistors (each transmission gate has two transistors and two transistors are used for inverting a clock signal. There are two transmission gates 50A and 50B, thus, six transistors are required). Thus, an RS-FF type circuit requires <sup>a fewer</sup> ~~less~~ number of transistors as far as a clock signal concerns, although an RS-FF type circuit requires <sup>a greater number</sup> ~~more~~ number of transistors ~~(in total)~~ than a transmission gate type circuit, and therefore, power consumption in an RS-FF type is smaller (C.Svensson and D.Liu, Low Power Design Methodologies, eds. J.M.Rabaey and M.Pedram (Kluwer Academic Publishers, 1996) <sup>Chap.3</sup> page 37).

The choice of an RS-FF type circuit or a transmission gate type circuit as a adiabatic charging reversible logic circuit should be designed base upon an object of a circuit, considering above analysis.

(The use in sub-threshold region)

6 7 In a specific condition, the current adiabatic charging register circuit can <sup>operate</sup> ~~operates~~ in weak inversion region with power supply voltage lower than threshold voltage (sub-threshold region;  $|V_{TP}| > V_{DD}$  and  $|V_{TN}| > V_{DD}$ ), like a prior CMOS circuit. It can be applied to slow speed operation LSI in sub-threshold region such as an environment sensor, or a living

body sensor.

3 (Effect of the invention)

As described above, according to an adiabatic charging register circuit of the present invention, power consumption consumed in a clock system is reduced approximately 1/10 of that of a conventional CMOS register circuit (Fig.16). Fig.16 shows that the power consumption by a clock signal and the power consumption of a logic circuit in <sup>the</sup> prior art are almost the same as each other, on the other hand, the power consumption by a clock signal in the present invention is only 1/10 of that of <sup>the</sup> prior art. Therefore, although the power consumption by a logic circuit in the present invention is the same as that of <sup>the</sup> prior art, the total power consumption including a clock system and a logic circuit in the present invention is considerably <sup>less</sup> smaller than that of <sup>the</sup> prior art.

Further, the present adiabatic charging register circuit is compatible with a conventional CMOS type register circuit. It is enough only to substitute an adiabatic charging type register circuit with a conventional CMOS type register circuit. Thus, the design of a circuit is quite simple.

From the foregoing, it should be appreciated that a new and improved adiabatic charging type register circuit has been found. It should be understood of course that the embodiments disclosed are merely illustrative and are not intended to limit the scope of the invention. Reference should be made to the appended claims, therefore, to indicate the scope of the invention.